# KamLAND register table of the front end electronics

*DRAFT*

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| Address (HEX) | read/write | Register name |
|---|---|---|
| 0 | r | Board ID (ASCII: ATWD) |
| 4 | r | Version: Board |
| 8 | r | Version: FPGA-VME |
| c | r | Version: FPGA-Channel |
| 10 | r | Memory size (MB) |
| 14 | r | Bank size (MB) |
| 200-37c | rw | DACs |
| 380 | rw | Test pulser ON/OFF (12 bit data word) |
| 384 | rw | retrigger time constant |
| 388 | rw | time to wait for global trigger after acquisition |
| 38c | rw | run ID 8 bit |
| 390 | rw | run ID 32 bit |
| 394 | rw | no level trigger on discriminator |
| 398 | rw | no discriminator launch of the ATWD (bit 0) |
| 3a0 | rw | *DEBUGGING ONLY!!* setting flag in channel FPGA |
| 3bc | rw | Reset channel FPGA |
| 400 | rw | Data start address |
| 404 | r | Data end address |
| 408 | rw | Bank number (bits 0-1) |
| 410 | r | busy (setting DACs & values to the channel) |
| 414 | rw | disable NSUM output (bit 0) |
| 420 | rw | channel enable (bits 0-11, one bit per channel) |
| 424 | rw | CSR (start/stop data taking, interrupt on/off) |
| 428 | rw | buffer fullness value for interrupt vector A (free space in kByte) |
| 42c | rw | interrupt vector A |
| 430 | rw | buffer fullness value for interrupt vector B (free space in kByte) |
| 434 | rw | interrupt vector B |
| 438 | rw | interrupt flag register. To be cleared by user |
| 43c | w | initialize buffer pointer (write $5A_{hex}$) |
| 440-46c | r | Frequency counter for discriminator hits |

Table 1: Register addresses

| Address (HEX) | Register name |
|---|---|
| 204 | Discriminator threshold channel 0 |
| 208 | Discriminator threshold channel 1 |
| 20c | Discriminator threshold channel 2 |
| 210 | Discriminator threshold channel 3 |
| 214 | Discriminator threshold channel 4 |
| 218 | Discriminator threshold channel 5 |
| 21c | Discriminator threshold channel 6 |
| 220 | Discriminator threshold channel 7 |
| 244 | Discriminator threshold channel 8 |
| 248 | Discriminator threshold channel 9 |
| 24c | Discriminator threshold channel 10 |
| 250 | Discriminator threshold channel 11 |
| 284 | Analog reference |
| 288 | ATWD Offset |
| 28c | Trigger bias current |
| 290 | Testpulser amplitude |
| 294 | Ramp top |

Table 2: DAC mapping

| Address (HEX) | Register name |
|---|---|
| 254 | Unused 2 4 |
| 258 | Unused 2 5 |
| 25c | Unused 2 6 |
| 260 | Unused 2 7 |
| 294 | Unused 3 4 |
| 29c | Unused 3 6 |
| 2a0 | Unused 3 7 |

Table 3: unused DAC mapping

| Address (HEX) | Register name |
|---|---|
| 440 | Channel 0 |
| 444 | Channel 1 |
| 448 | Channel 2 |
| 44c | Channel 3 |
| 450 | Channel 4 |
| 454 | Channel 5 |
| 458 | Channel 6 |
| 45c | Channel 7 |
| 460 | Channel 8 |
| 464 | Channel 9 |
| 468 | Channel 10 |
| 46c | Channel 11 |

Table 4: Frequency counter mapping

| Bit | Function |
|---|---|
| 0 | Data taking ON/OFF (1=ON,0=OFF) |

Table 5: CSR (Control and Status Register)

| Address | Bit | Function |
|---|---|---|
| 4f8 | 0 | ATWD power (5V) ON/OFF (1=ON,0=OFF) |
| 4fc | 1-0 | Testpulser H gain (bit 0=continous, bit 1=40MHz) |
| 4fc | 9-8 | Testpulser M gain (bit 8=continous, bit 9=40MHz) |
| 4fc | 17-16 | Testpulser L gain (bit 16=continous, bit 17=40MHz) |
| 4fc | 25-24 | Testpulser C (Clock)(bit 24=continous, bit 25=40MHz) |

Table 6: *OLD* ATWD test registers

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