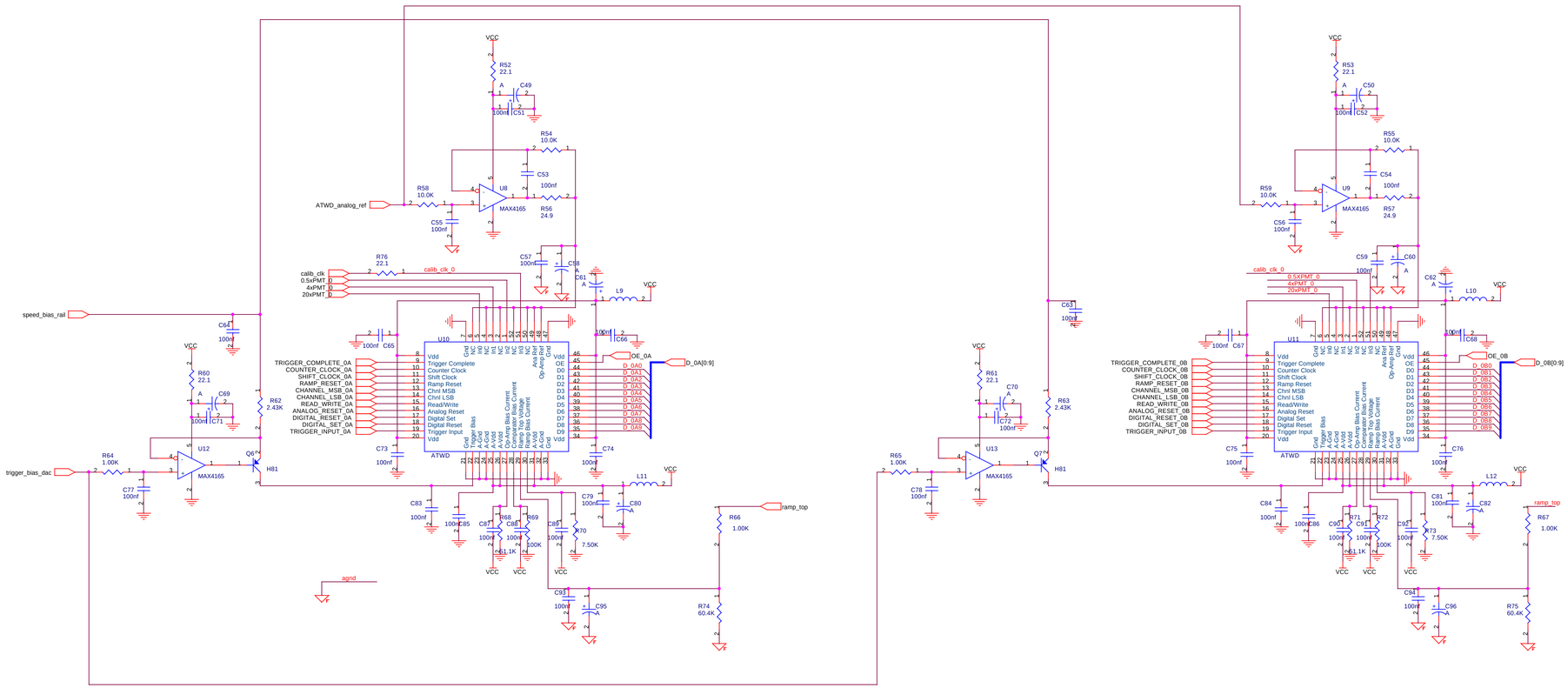


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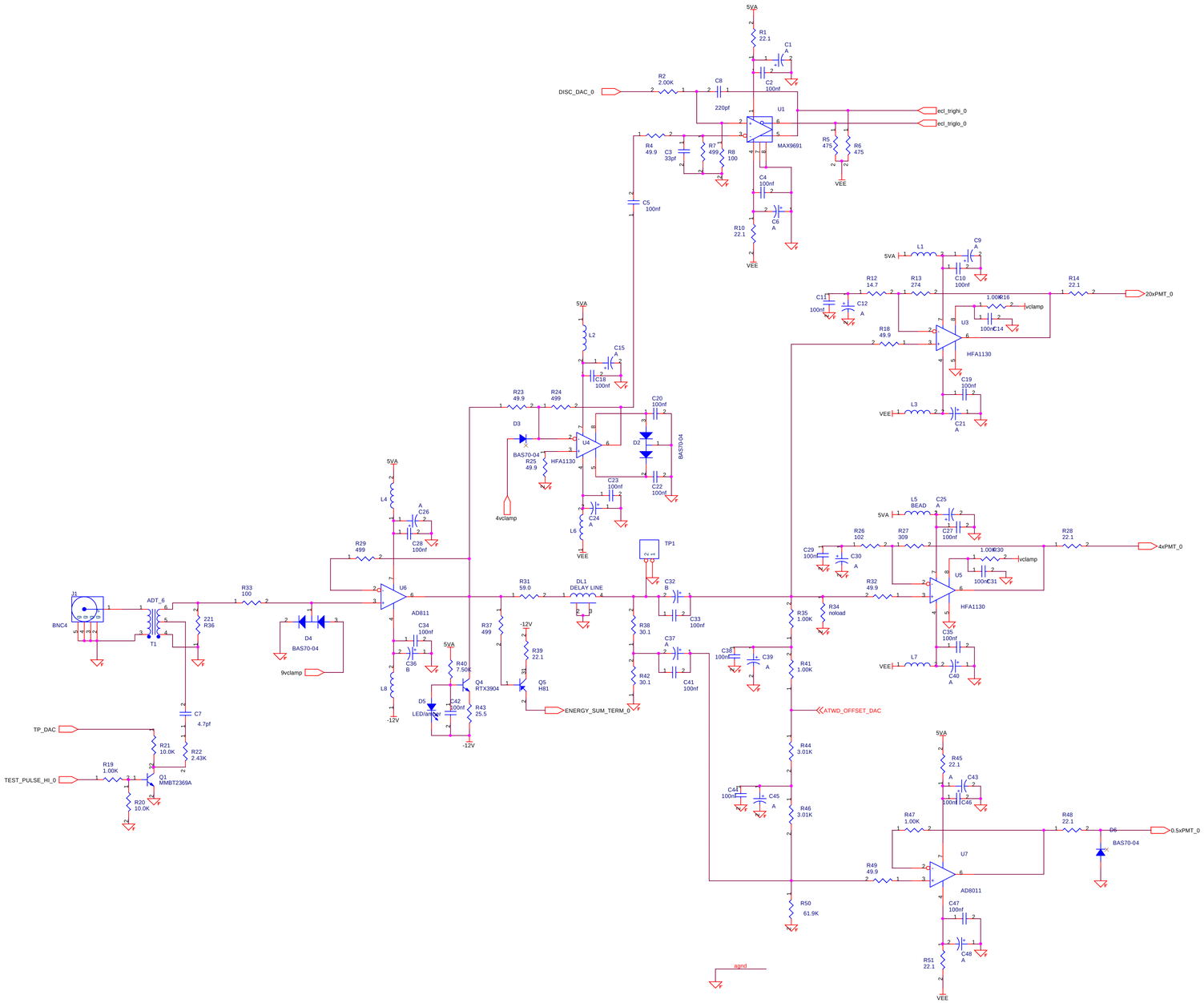
Date: Wednesday, July 25, 2001 | Sheet 1 of 14

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| Revisions: | Lawrence Berkeley National Laboratory |
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| Designer: **Bieser** | Project: **KAM LAND** |
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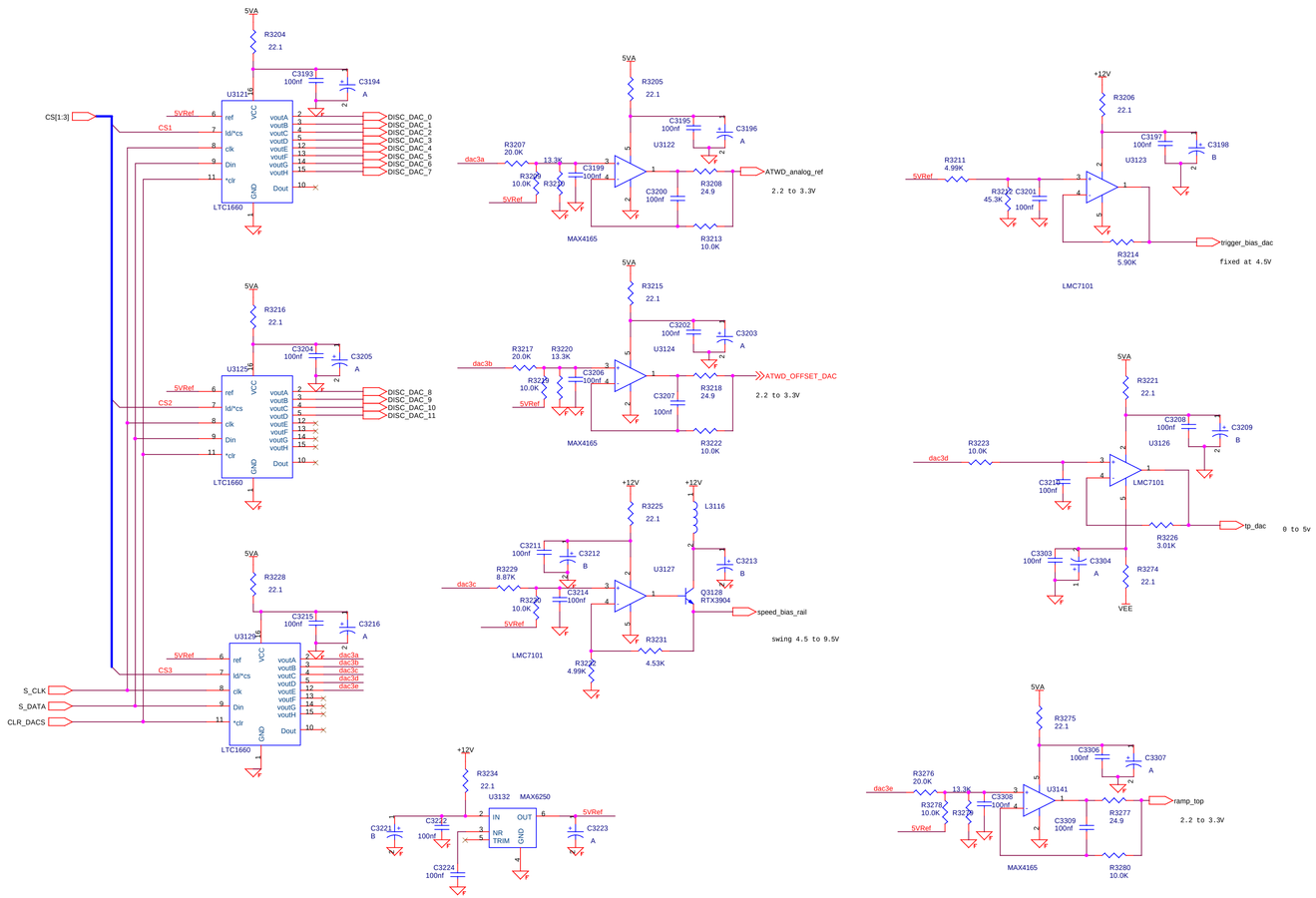


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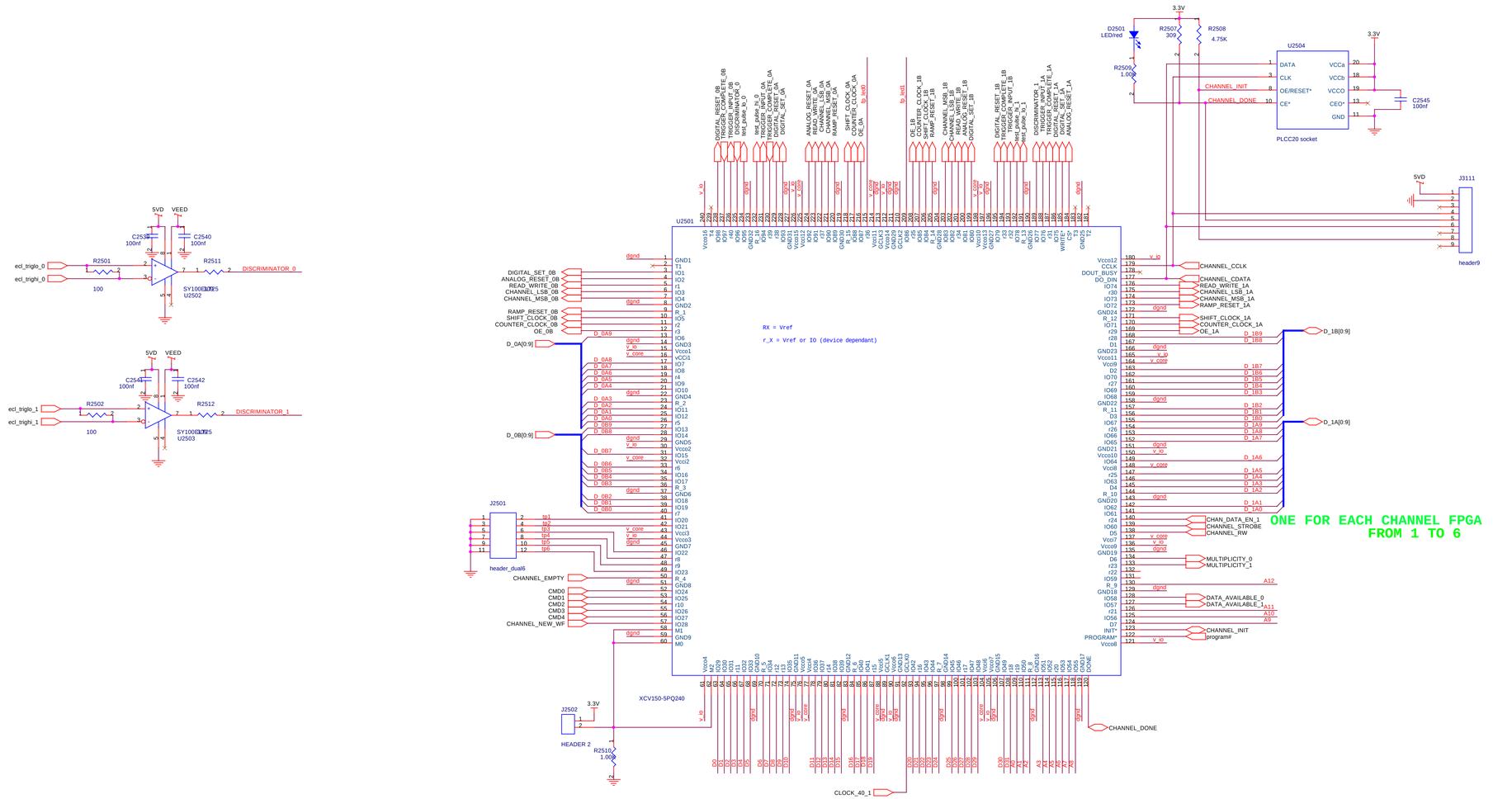


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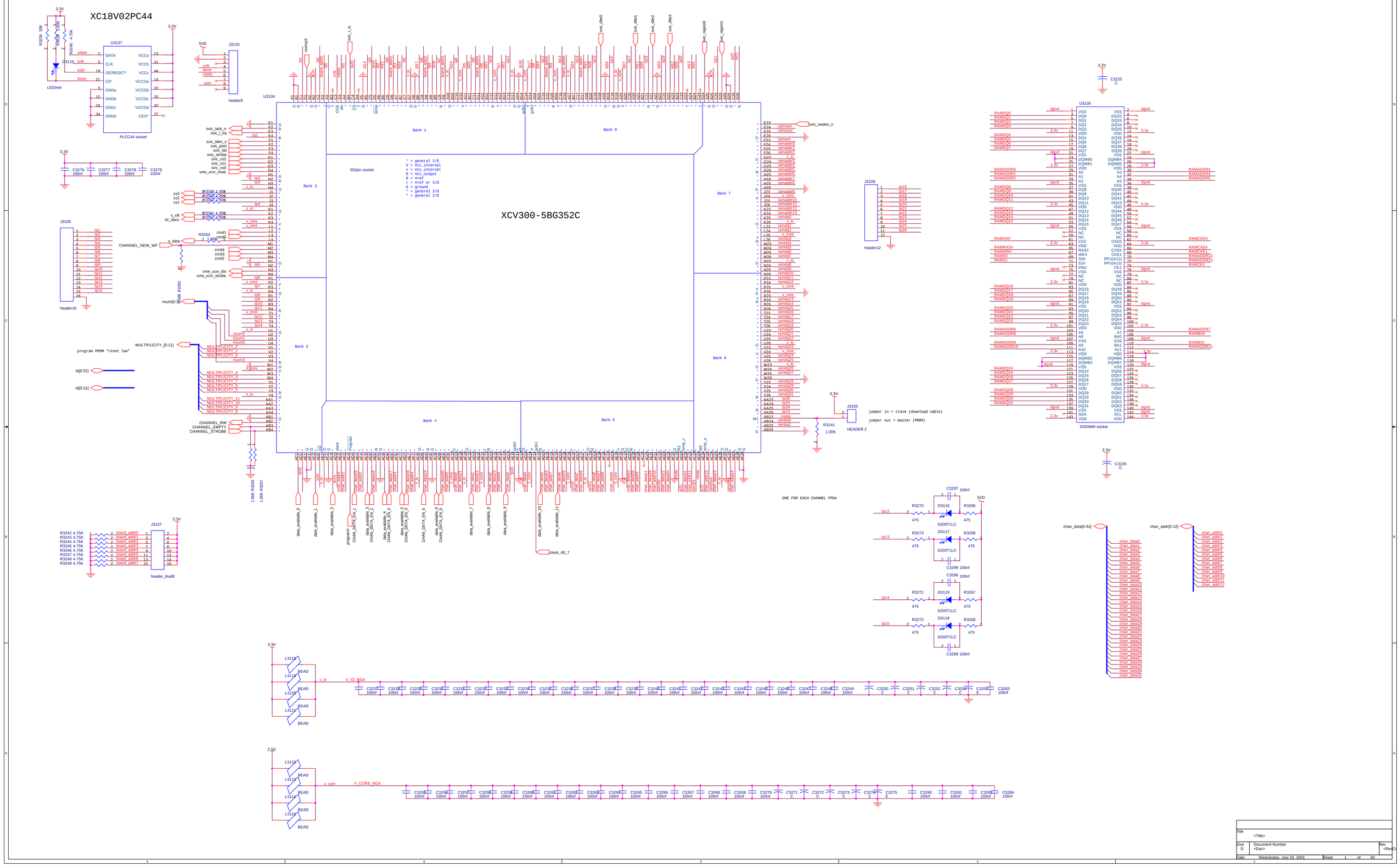
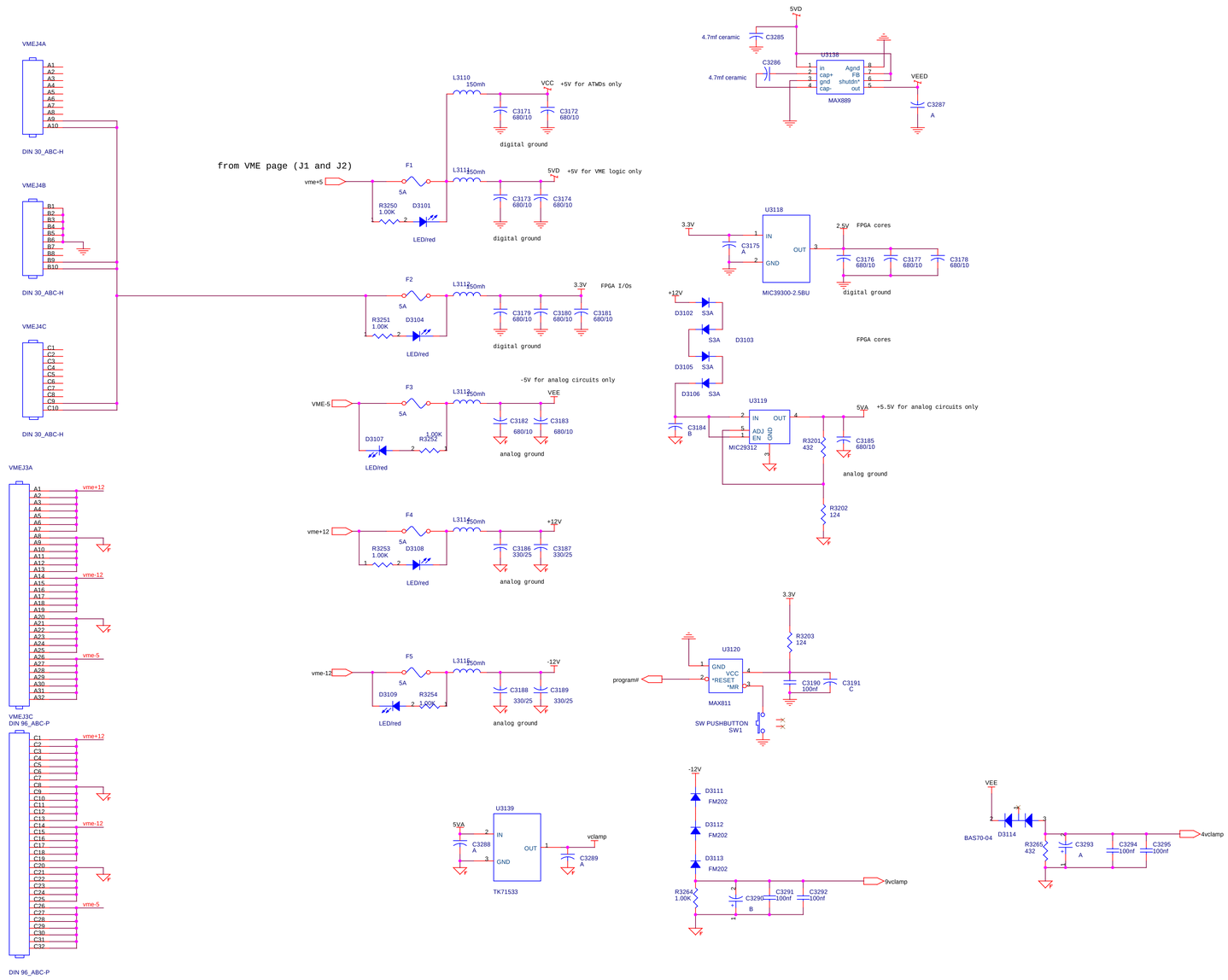

XC18V02PC44
U3137
PLCC44 socket
U3134
XCV300-5BG352C
352pin socket
Bank 0
Bank 1
Bank 2
Bank 3
Bank 4
Bank 5
Bank 6
Bank 7
* = general I/O
V = Vcc_internal
v = Vcc_internal
O = Vcc_output
R = Vref
r = Vref or I/O
G = ground
* = general I/O
* = general I/O
* = general I/O
J3108
header16
J3110
header9
J3109
header12
J3105
HEADER 2
jumper in = slave (download cable)
jumper out = master (PROM)
U3135
SODIMM socket
J3107
header_dual8
ONE FOR EACH CHANNEL FPGA
program PROM "reset low"
CHANNEL_NEW_WF
MULTIPLICITY_[0:11]
CHANNEL_RW
CHANNEL_EMPTY
CHANNEL_STROBE
clock_40_7
chan_data[0:31]
chan_addr[0:12]
V_IO_BGA
V_CORE_BGA

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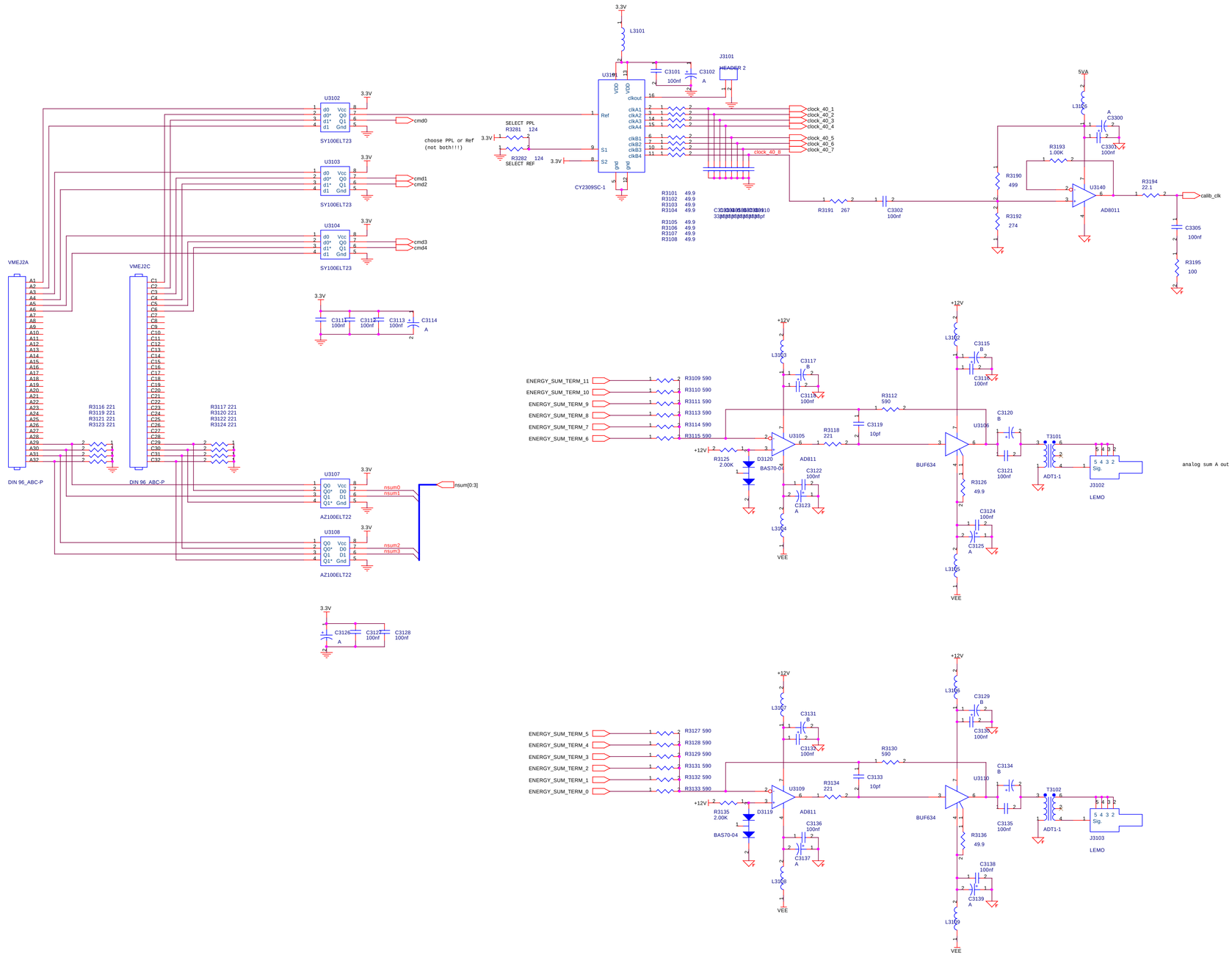


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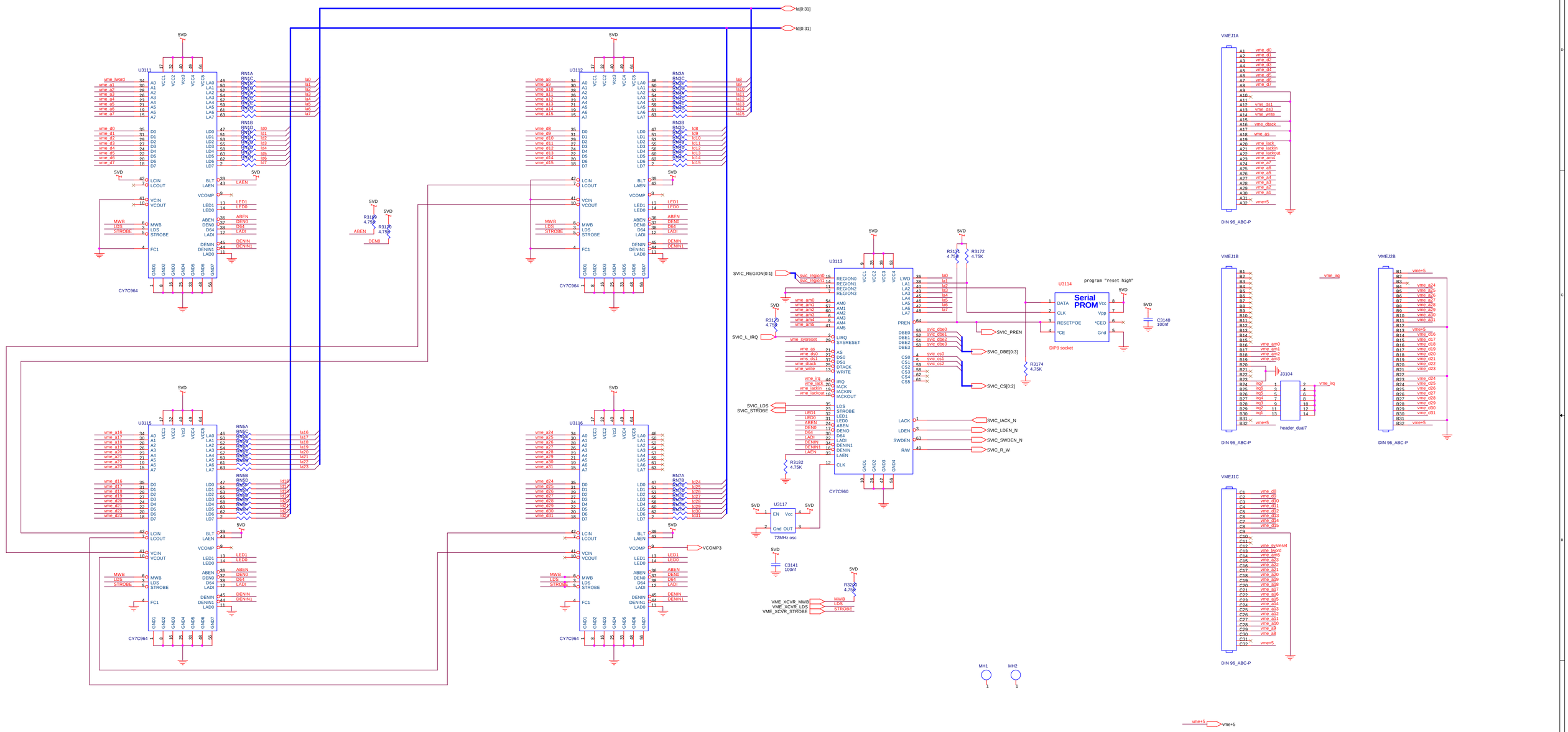


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